

Claims

1 1. A structure comprising:
2 a first substrate and a second substrate; and
3 first solder bumps and second solder bumps
4 therebetween, wherein said second solder bumps have at
5 least a portion that melts at a substantially lower
6 temperature than said first solder bumps.

1 2. A structure as recited in claim 1, wherein said
2 second solder bumps are larger than said first solder bumps.

1 3. A structure as recited in claim 1, wherein said
2 second solder bumps comprise a portion having a higher
3 concentration of tin than does said first solder bumps.

1 4. A structure as recited in claim 3, wherein said
2 portion comprises a eutectic concentration of tin.

1 5. A structure as recited in claim 3, wherein said
2 portion is adjacent to said second substrate.

1 6. A structure as recited in claim 3, wherein said
2 portion is centrally located within said second solder bump.

1 7. A structure as recited in claim 3, wherein said
2 portion is said entire second solder bumps.

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Sub 9,
and 1.

8. A structure as recited in claim 1, wherein said second solder bumps are for aligning said first substrate and said second substrate before melting said first solder bumps.

9. A structure as recited in claim 8, wherein said second solder bumps are larger than said first solder bumps.

10. A structure as recited in claim 1, wherein said second solder bumps melt at a temperature at least 25C less than said first solder bumps.

11. A structure as recited in claim 1, wherein said first substrate comprises a first semiconductor chip.

12. A structure as recited in claim 11, wherein said second substrate comprises a second semiconductor chip.

13. A structure as recited in claim 12, wherein said second chip is larger than said first chip.

14. A structure as recited in claim 12, wherein said second chip further comprises wire bond pads for bonding to a printed circuit board.

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1 15. A method of joining, comprising:

2 (a) providing a first substrate and a second
3 substrate; and

4 (b) providing first solder bumps and second
5 solder bumps connecting said first substrate
6 and said second substrate, wherein said
7 second solder bumps have at least a portion
8 that melts at a substantially lower
9 temperature than said first solder bumps.

1 16. A method as recited in claim 15, wherein said
2 providing (b) comprises providing said second solder bumps
3 larger than said first solder bumps.

1 17. A method as recited in claim 15, wherein said
2 providing (b) comprises providing said second solder bumps
3 with a portion having a higher concentration of tin than
4 said first solder bumps.

1 18. A method as recited in claim 17, wherein said
2 portion comprises a eutectic concentration of tin.

1 27. A method as recited in claim 26, wherein said
2 second substrate comprises a second semiconductor chip.

1 28. A method as recited in claim 27, wherein said
2 second chip is larger than said first chip.

1 29. A method as recited in claim 28, wherein said
2 second chip further comprises wire bond pads for bonding to
3 a printed circuit board.

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